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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/612,872
Filing Date	July 7, 2003
First Named Inventor	Terry DISHONGH et al.
Art Unit	2831
Examiner Name	Nguyen T. HA
Attorney Docket Number	Intel 2207/807702

Total Number of Pages in This Submission: 11

ENCLOSURES *(Check all that apply)*

- [✔] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment/Reply
- [ ] After Final
- [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
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- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [✔] Other Enclosure(s) (please Identify below):
  1. **Certificate of Correction**
  2. **Copy of Patent 7,057,114 with changes marked in red**

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Sumit Bhattacharya (Reg. No. 51,469)
Signature	Sumit Bhattacharya
Date	October 25, 2006

CERTIFICATE OF TRANSMISSION/MAILING

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Patent

Attorney Docket No.: 2207/807702
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS	:	Terry DISHONGH et al.
SERIAL NO.	:	10/612,872
FILED	:	July 7, 2003
PATENT NO.	:	7,057,114 B2
ISSUED	:	June 6, 2006
FOR	:	CIRCUIT BOARD WITH ADDED IMPEDANCE

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Pilar Rodriguez

REQUEST FOR CERTIFICATE OF CORRECTION

Dear Sir:

We have compared the above patent with the application as filed and have found errors in the printing of the patent. We respectfully request that the enclosed Certificate of Correction on Form PTO-1050 be issued correcting the mistakes set forth therein under authority of 35 U.S.C. §254. The exact column and line number where the errors occurred in the patent are listed on the enclosed certificate.

11/01/2006 MBELETE1 00000070 110600 7057114
01 FC:1811 100.00 DA

The errors that appear in the patent are typographical errors made by the Applicant and therefore, a fee is required.

Please charge payment of the Certificate of Correction fee of $100.00 to Deposit Account No. **11-0600.** The office is hereby authorized to charge any additional fees, or credit any overpayments, to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON

Dated: October 25, 2006

By: _____
Sumit Bhattacharya
(Reg. No. 51,469)

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : **7,057,114 Bs**

DATED : **June 6, 2006**

INVENTOR(S) : **Terry DISHONGH et al.**

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2, Line 64: "said first said"
should be: --said first cap--

MAILING ADDRESS OF SENDER: **Attorney Ref.: Intel 2207/807702**
Kenyon & Kenyon LLP
333 W. San Carlos St., Suite 600
San Jose, CA 95110
Telephone: (408) 975-7600

PATENT NO. **7,057,114 B2**

Date: October 25, 2006

No. of additional copies

PTO/SB/17 (10-04v2)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

FEE TRANSMITTAL for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **100.00**

Complete if Known	
Application Number	10/612,872
Filing Date	July 7, 2003
First Named Inventor	Terry DISHONGH et al.
Examiner Name	Nguyen T. HA
Art Unit	2831
Attorney Docket No.	2207/807702

METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☒ Deposit Account:

Deposit Account Number: **11-0600**

Deposit Account Name: **Kenyon & Kenyon LLP**

The Director is authorized to: *(check all that apply)*
☒ Charge fee(s) indicated below ☒ Credit any overpayments
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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	790	2001	395	Utility filing fee	
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filling fee	
				SUBTOTAL (1)	($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below		Fee Paid
Total Claims		=		X	=	
Independent Claims		=		X	=	
Multiple Dependent				X	=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple dependent claim, if not paid
1204	200	2204	100	** Reissue independent claims over original patent
1205	50	2205	25	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	500	2452	250	Petition to revive – unavoidable	
1453	1,500	2453	750	Petition to revive – unintentional	
1501	1,400	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17 (q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	
				Other fee (specify) **Certificate Of Correction**	100.00

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 100.00

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Sumit Bhattacharya	Registration No. (Attorney/Agent)	51,469	Telephone	(408) 975-7500
Signature	Sumit Bhattacharya			Date	October 25, 2006

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US007057114B2

(12) United States Patent
Dishongh et al.

(10) Patent No.: US 7,057,114 B2
(45) Date of Patent: *Jun. 6, 2006

(54) CIRCUIT BOARD WITH ADDED IMPEDANCE

(75) Inventors: **Terry Dishongh**, Hillsboro, OR (US); **Prateek Dujari**, Portland, OR (US); **Bin Lian**, Hillsboro, OR (US); **Damion Searls**, Portland, OR (US)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 88 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/612,872**

(22) Filed: **Jul. 7, 2003**

(65) **Prior Publication Data**

US 2004/0057184 A1 Mar. 25, 2004

Related U.S. Application Data

(63) Continuation of application No. 09/473,128, filed on Dec. 28, 1999, now Pat. No. 6,775,122.

(51) **Int. Cl.**
H05K 1/00 (2006.01)

(52) **U.S. Cl.** **174/250**; 174/260; 174/262; 361/306.1; 361/306.3; 361/311; 361/313; 361/704; 361/761

(58) **Field of Classification Search** 174/260, 174/250, 262; 361/311, 313, 321.1, 303, 361/306.3, 704, 761, 306.1
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,473,312	B1 *	10/2002	Hiratsuka et al.	361/794
6,602,078	B1 *	8/2003	Kwark	439/66
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6,761,816	B1 *	7/2004	Blackburn et al.	205/777.5
6,775,122	B1 *	8/2004	Dishongh et al.	361/301.5

FOREIGN PATENT DOCUMENTS

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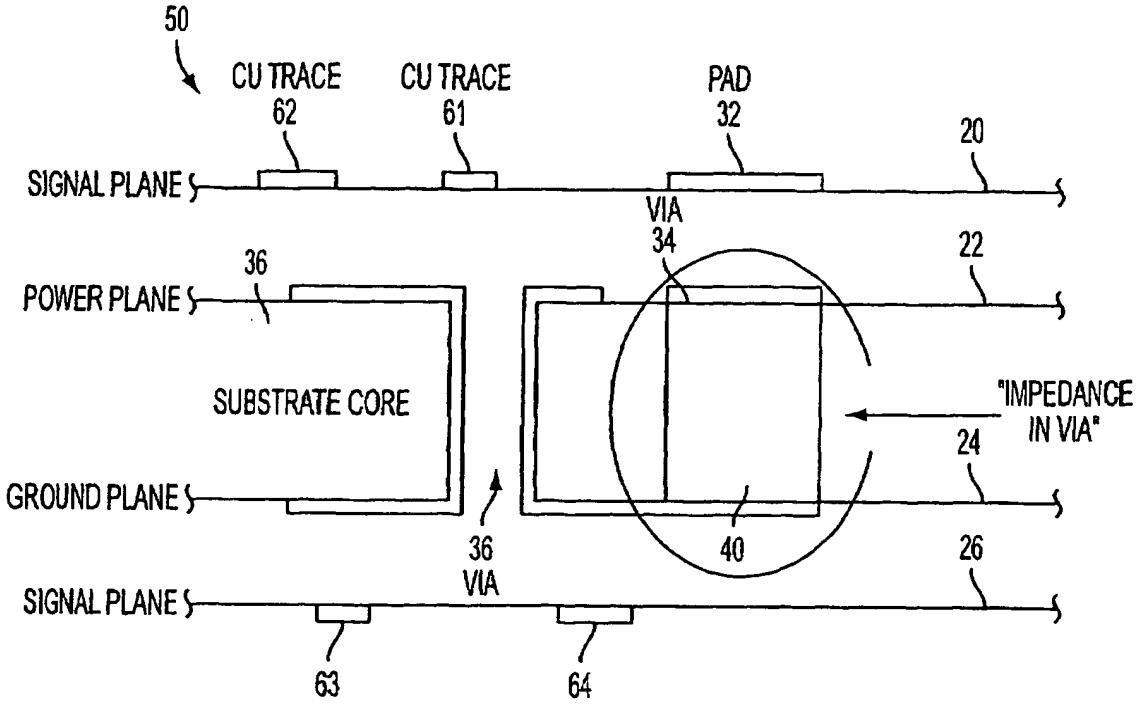
* cited by examiner

Primary Examiner—Nguyen T. Ha
(74) *Attorney, Agent, or Firm*—Kenyon & Kenyon LLP

(57) **ABSTRACT**

A circuit board includes two planes. A via spans the planes, and an impedance component is placed in the via. The impedance component is coupled to both of the planes. The impedance component provides an impedance between the planes without the use of traces or hand soldering of components.

5 Claims, 2 Drawing Sheets



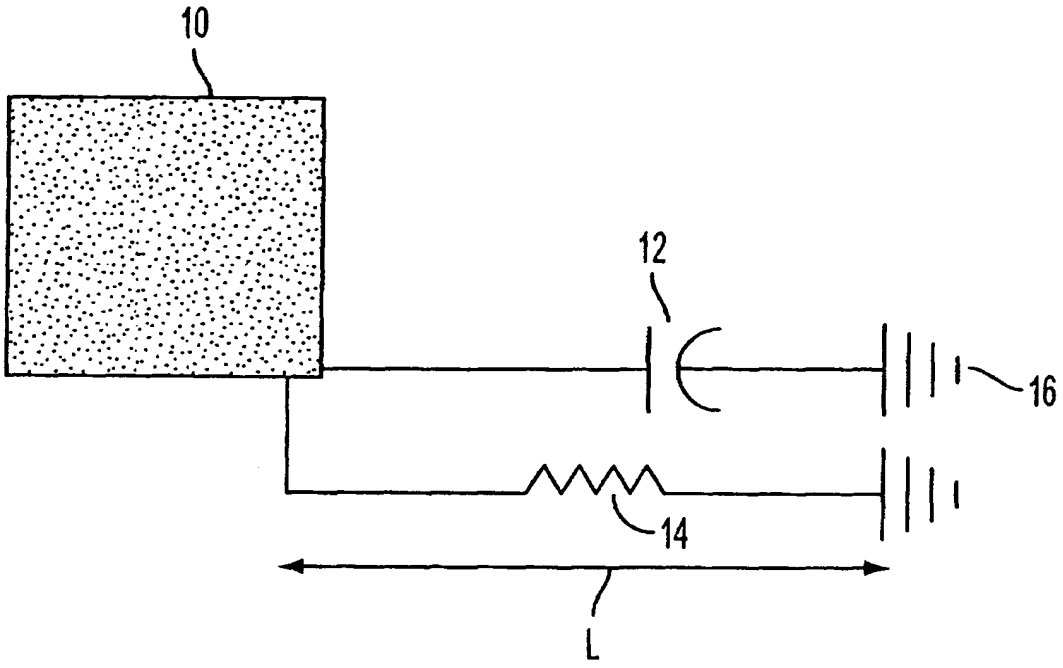


FIG. 1
(PRIOR ART)

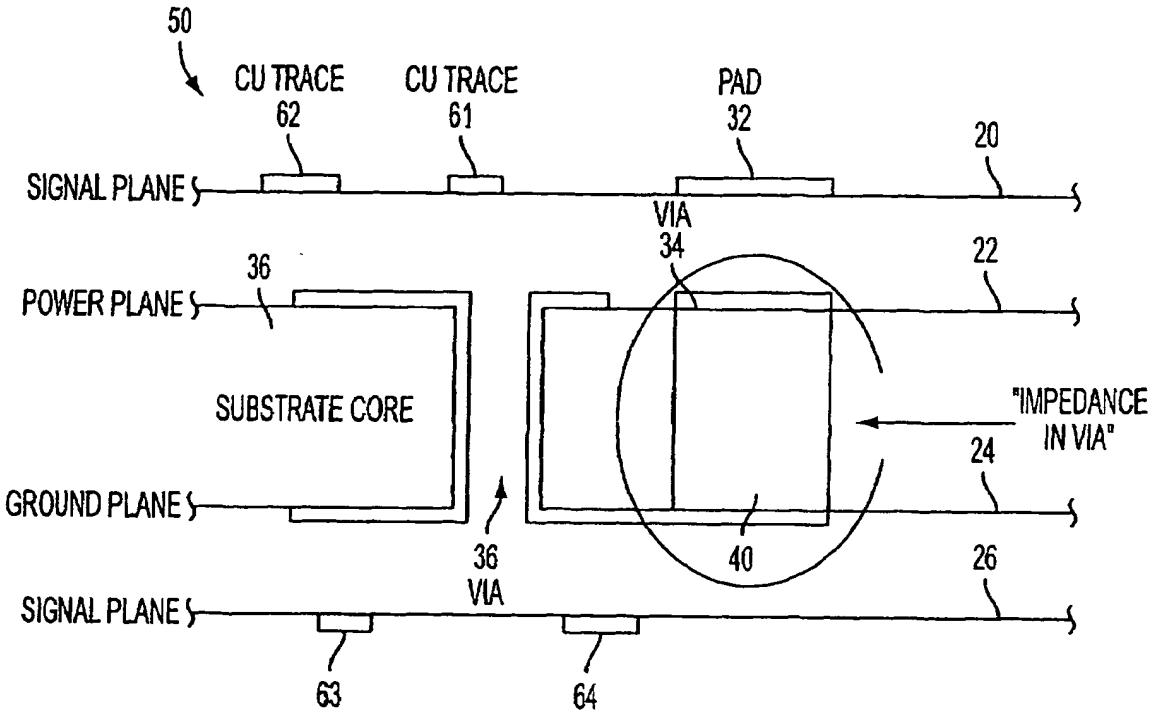

50
CU TRACE
62
CU TRACE
61
PAD
32
20
SIGNAL PLANE
VIA
34
22
36
POWER PLANE
SUBSTRATE CORE
"IMPEDANCE IN VIA"
24
GROUND PLANE
36
VIA
40
26
SIGNAL PLANE
63
64

FIG. 2

CIRCUIT BOARD WITH ADDED IMPEDANCE

This application is a continuation of application Ser. No. 09/473,128 filed Dec. 28, 1999 now U.S. Pat. No. 6,775,122.

FIELD OF THE INVENTION

The present invention is directed to semiconductor devices and electronic circuit boards. More particularly, the present invention is directed to added impedance in semiconductor devices and electronic circuit boards.

BACKGROUND OF THE INVENTION

Current designs of semiconductor circuits require certain impedances between the power plane and the ground plane. These impedances are generally placed on the die or on the substrate of the circuitry. For example, decoupling capacitors are typically placed in circuits, between the power plane and ground plane, to stabilize any undue voltage fluctuations in the traces. Similarly, resistances may also be used at various locations in circuits to add impedance.

FIG. **1** illustrates a semiconductor circuit with added impedance using known methods. Between a power plane **10** and ground **16**, a surface mount capacitor **12** and a surface mount resistor **14** is added. Capacitor **12** and resistor **14** are usually hand-soldered on the substrate requiring additional resources. They also occupy precious real estate on the substrate. In addition, due to the considerable length of the trace (L) between power plane **10** and ground **16**, the trace can act as an antenna for electromagnetic interference ("EMI") and other high frequency noises.

Based on the foregoing, there is a need for an improved method and apparatus for adding impedance between planes in a semiconductor circuit.

SUMMARY OF THE INVENTION

One embodiment of the present invention is a circuit board that includes two planes. A via spans the planes, and an impedance component is placed in the via. The impedance component is coupled to both of the planes.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates in a semiconductor circuit with added impedance using known methods.

FIG. **2** illustrates a circuit board in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

One embodiment of the present invention is a circuit board that includes impedance components inserted in the vias between two planes.

FIG. **2** illustrates a circuit board **50** in accordance with one embodiment of the present invention. Circuit board **50** includes four layers: signal planes **20** and **26**; a power plane **22**; and a ground plane **24**. Power plane **22** and ground plane **24** are sandwiched around a substrate core **36**. Circuit board **50** further includes a pad **32**, and copper ("Cu") traces **61–64**. Finally, circuit board **50** includes multiple vias **34** and **36** that are openings spanning two or more planes.

In order to add impedance between planes of circuit board **50**, an impedance component is inserted inside a via and coupled to each of the planes. An impedance component is a circuit device that adds impedance, such as a resistor or a capacitor. In the example shown in FIG. **2**, an impedance component **40** is placed inside via **34** and connects power plane **22** directly to ground plane **24**.

If a resistance impedance is desired, in one embodiment a resistor is formed by rolling carbon material into a cylinder of approximately the same diameter as via **34**. The "roll" is then cut into the desired height approximating the height of via **34**, and is capped with conductive material. The resistor roll is then press fitted into via **34** using, for example, forced air, and each cap is coupled to one of the planes.

If a capacitance impedance is desired, in one embodiment a capacitor is formed by rolling a sandwich of a dielectric material on top of conductive material to the desired diameter. The "roll" is then cut to the desired height, and the interior and exterior of the roll is capped. The capacitor roll is then press fitted into via **34** and each cap is coupled to one of the planes.

By placing an impedance component in a via of a circuit board, various advantages over prior art methods of adding impedance are achieved. The advantages include: eliminating the process of hand soldering the capacitor/resistor; not occupying any real estate on the circuit board; and eliminating high frequency noise that would otherwise be picked up by a trace.

As described, the present invention places impedance components in vias of a circuit board in order to add impedance between planes. This eliminates many problems associated with adding impedance through trace lines and hand soldiered components.

Several embodiments of the present invention are specifically illustrated and/or described herein. However, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.

For example, although a four layer circuit board is illustrated, any number of layers can utilize the invention in order to add impedance between two of the layers.

What is claimed is:

1. A circuit board comprising:

a first plane;

a second plane;

a via spanning said first and second plane; and

an impedance component placed in said via and coupled to said first plane and said second plane further comprising rolled carbon material having a first end and a second end.

2. The circuit board of claim **1**, wherein said impedance component is a resistor.

3. The circuit board of claim **2**, wherein said resistor comprises:

a first conductive cap coupled to said first end, and a second conductive cap coupled to said second end;

wherein said first conductive cap is coupled to said first plane, and said second conductive cap is coupled to said second plane.

4. A method of adding impedance to a circuit board having a first plane, a second plane, and a via spanning said first and second plane, said method comprising:

forming an impedance component having a first conductive cap and a second conductive cap;

placing said impedance component in said via; and

coupling ~~said first said~~ to said first plane and said second cap to said second plan wherein said impedance component further comprises; rolled carbon material having a first end and a second end.

Said first cap

5. A circuit board comprising:

a plurality of planes;

a via spanning at least two of said planes; and

an impedance component placed in said via and coupled to at least two of said planes wherein said impedance component is a resistor further comprising:

rolled carbon material having a first end and a second end: and

a first conductive cap coupled to said first end, and

a second conductive cap coupled to said second end;

wherein said first conductive cap is coupled to said first plane, and said second conductive cap is coupled to said second plane.

* * * * *